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Dated: August 31, 2004

Signature: 

(Marcus J. Millet)

Docket No.: TESSERA 3.0-297  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:  
Masud Beroz

Application No.: 10/600,186

Group Art Unit: 2811

Filed: June 20, 2003

Examiner: J. M. Im

For: SIMPLIFIED STACKED CHIP  
ASSEMBLIES

**RESPONSE TO RESTRICTION REQUIREMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

This communication is in response to the Official Action mailed July 14, 2004, setting forth a Restriction Requirement in the above-identified application. A petition for a one-month extension of the term for response to said Official Action, to and including September 14, 2004, is transmitted herewith.

In the Official Action, the Examiner required restriction to one of the following inventions under 35 U.S.C. § 121:

- I. Claims 1-15, drawn to a semiconductor device.
- II. Claims 16-19, drawn to a method of fabricating a semiconductor device.

In response, Applicants hereby elect the invention of Group I, corresponding to claims 1-15 for prosecution in this

case. Applicants reserve the right to file a divisional application corresponding to the non-elected claims.

In the event any fee is due in connection with the present response, the Examiner is authorized to charge Applicant's Deposit Account No. 12-1095 therefor.

Dated: August 31, 2004

Respectfully submitted,

By 

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